Attorney Docket No.: 0180151

IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Labelle, et al.**	Art Unit: 1765
Serial No.: 10/705,347	Examiner: Chen, Kin-Chan
Filed: November 8, 2003	
For: **Method for Integrating a High-K Gate Dielectric in a Transistor Fabrication Process**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1, 6-8, 14-16, and 19-20. The Final Rejection issued on December 7, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on March 3, 2006.

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REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1, 6-8, 14-16, and 19-20 are pending, and claims 2-5, 9-13, and 17-18 were canceled in previous amendments. Claims 1, 6-8, 14-16, and 19-20 have been finally rejected in a Final Rejection dated December 7, 2005. This Appeal is directed to the rejection of claims 1, 6-8, 14-16, and 19-20. Claims 1, 6-8, 14-16, and 19-20 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments have been entered after issuance of the Final Rejection of December 7, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 defines a method for forming a field-effect transistor on a substrate (e.g., substrate 104 in Figure 1). The substrate (e.g., substrate 104 in Figure 1) includes a high-k dielectric layer (not shown in Figure 1) situated over the substrate and a gate electrode layer (not shown in Figure 1) situated over the high-k dielectric layer. *See*, e.g., page 7, lines 14-16 and Figure 1of the present application.

The method includes the step of etching (e.g., step 202 of flowchart 200 in Figure 2) the gate electrode layer (not shown in Figure 1) and the high-k dielectric layer (not shown in Figure 1) in a plasma process chamber to form a gate stack (e.g., gate stack 102 in Figure 1). *See*, e.g., page 7, lines 12-14 and 16-18 and Figures 1 and 2 of the present application. The gate stack (e.g., gate stack 102 in Figure 1) includes a high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1) situated over the substrate (e.g., substrate 104 in Figure 1) and a gate electrode segment (e.g., gate electrode segment 108 in Figure 1) situated over the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1).

Thereafter, a nitridation process (e.g., step 204 of flowchart 200 in Figure 2) utilizing a nitrogen containing plasma is performed on the gate stack (e.g., gate stack 102 in Figure 1) in the plasma process chamber to nitridate the sidewalls (e.g., sidewalls 110 in Figure 1) of the gate stack (e.g., gate stack 102 in Figure 1). *See*, e.g., page 7, lines 18-

22, page 8, lines 1-2 and Figure 1 of the present application. The nitridation process performed on the gate stack (e.g., gate stack 102 in Figure 1) causes nitrogen to enter the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1), thereby allowing the nitrogen to form an oxygen diffusion barrier in the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1). *See*, e.g., page 8, lines 14-18 and Figure 1 of the present application.

B. Claim 8

Independent claim 8 defines a method for forming a field-effect transistor on a substrate substantially similar to that defined by independent claim 1, with the additional step of selecting the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1) from the group consisting of hafnium oxide, hafnium silicate, zirconium oxide, zirconium silicate, and aluminum oxide. *See*, e.g., page 6, line 22, page 7, lines 1-2, and Figure 1 of the present application.

C. Claim 15

Independent claim 15 defines a method for forming a field-effect transistor on a substrate (e.g., substrate 104 in Figure 1). The substrate (e.g., substrate 104 in Figure 1) includes a high-k dielectric layer (not shown in Figure 1) situated over the substrate and a gate electrode layer (not shown in Figure 1) situated over the high-k dielectric layer. *See*, e.g., page 7, lines 14-16 and Figure 1of the present application.

The method includes the step of etching (e.g., step 202 of flowchart 200 in Figure 2) the gate electrode layer (not shown in Figure 1) and the high-k dielectric layer (not shown in Figure 1) in a plasma process chamber to form a gate stack (e.g., gate stack 102 in Figure 1). *See*, e.g., page 7, lines 12-14 and 16-18 and Figure 1 of the present application. The gate stack (e.g., gate stack 102 in Figure 1) includes a high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1) situated over the substrate (e.g., substrate 104 in Figure 1), a gate electrode segment (e.g., gate electrode segment 108 in Figure 1) situated over the high-k dielectric segment (e.g., high-k dielectric segment 106 in Figure 1), and includes sidewalls (e.g., sidewalls 110 in Figure 1).

Thereafter, a nitrogen plasma is utilized to nitridate (e.g., step 204 of flowchart 200 in Figure 2) the sidewalls (e.g., sidewalls 110 in Figure 1) of the gate stack (e.g., gate stack 102 in Figure 1) in the plasma process chamber. *See*, e.g., page 7, lines 19-22, page 8, lines 1-2, and Figure 1 of the present application. Source/drain regions are then formed adjacent to the gate stack (e.g., gate stack 102 in Figure 1) and spacers are fabricated on the sidewalls (e.g., sidewalls 110 in Figure 1) of the gate stack. *See*, e.g., page 9, line 2-3 of the present application. A rapid thermal anneal is then performed on the gate stack (e.g., gate stack 102 in Figure 1). *See*, e.g., page 9, lines 3-4 of the present application.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 6-8, 14-16, and 19-20 under 35 USC §103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0079696 to Colombo (hereinafter "Colombo") in view of U.S. Patent No. 6,265,260 to Alers et al. (hereinafter "Alers"), or U.S. Patent No. 6,566, 250 to Tu et al. (hereinafter "Tu") as evidenced by U.S. Patent Application Publication No. 2004/0188240 to Chang et al. (hereinafter "Chang '240"), or U.S. Patent No. 6,090,210 to Ballance et al. (hereinafter "Ballance"), or U.S. Patent No. 6,759,337 to Aronowitz et al. (hereinafter "Aronowitz"), or U.S. Patent Application Publication No. 2005/0019964 to Chang et al. (hereinafter "Chang '964").

B. Claims 1, 6-8, 14-16, and 19-20 under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,891,798 to Doyle et al. (hereinafter "Doyle") in view of Alers, or Tu as evidenced by Chang '240, or Ballance, or Aronowitz, or Chang '964.

ARGUMENT

A. Rejection of Claims 1, 6-8, 14-16, and 19-20 Under 35 USC §103(a) as Being Unpatentable Over Colombo in View of Alers, or Tu as Evidenced by Chang '240, or Ballance, or Aronowitz, or Chang '964.

Appellants respectfully submit that the present invention, as defined by independent claims 1, 8, and 15, is patentably distinguishable over the cited references, either singly or in combination.

By reference to Figures 1 and 2 of the present application, the present invention performs a nitridation process on gate stack 102 immediately after the gate etch process has been performed. By performing the nitridation process to nitridate sidewalls 110 of gate stack 102 after the gate etch process has been performed, the present invention's process flow can utilize the nitridation process to repair damage that may occur to gate stack 102 during the gate etch process. Additionally, during the nitridation process, nitrogen is introduced into high-k dielectric segment 106. As a result, the nitrogen that is introduced into high-k dielectric segment 106 can form a barrier that can prevent undesirable lateral oxygen diffusion into high-k dielectric segment 106 during subsequent processing steps. In an embodiment of the present invention that utilizes a gate stack comprising an interfacial layer, where the interfacial layer comprises nitride, the nitridation process can also replace nitride that has been depleted in the interfacial layer during the gate etch process. *See*, e.g., page 8 of the present application, lines 9-21. Moreover, as required by the independent claims, the processes of etching the gate stack

and the nitridation of the etched gate stack are performed in a single process chamber. *See*, e.g., page 9 of the present application, lines 20-22. Utilization of a single process chamber has a number of advantages; for example, there will be no need to break vacuum and, thus, throughput is increased and manufacturing costs are reduced.

Colombo describes encapsulated MOS transistor gate structures and methods for making the same. According to Colombo, sidewalls of patterned gate structures are conditioned by nitriding the sidewalls of the gate structure, and a silicon nitride encapsulation layer is formed to protect the conditioned sidewalls during manufacturing processing. The conditioning and encapsulation avoid oxidation of metal gate layers, and also facilitate repairing or restoring stoichiometry of metal that may be damaged or altered during gate patterning. *See*, Figures 4, and 5G through 5L of Colombo.

However, as the Examiner has acknowledged, Colombo does not teach, disclose, or suggest utilizing plasma, much less using the same plasma chamber for both the gate etch and nitridation processes as disclosed and claimed by the present invention. *See*, e.g., page 4 of the present Office Action, lines 5-7. However, the Examiner has stated that any of the cited references Alers or Tu can be used to cure this deficiency of Colombo, as evidenced by Chang '240, Ballance, Aronowitz, or Chang '964. *See*, e.g., page 3 of the present Office Action, lines 12-17.

Alers is directed to a method for making a capacitor by forming a first metal electrode comprising a metal nitride surface and a tantalum pentoxide layer on the metal nitride surface while maintaining a temperature below an oxidizing temperature of the

metal, and remote plasma annealing the tantalum pentoxide layer. *See*, e.g., column 1, line 62 through column 2, line 54 of Alers. Thus, Alers does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch.

Moreover, Tu is directed to forming a self-aligned capping layer over a metal filled feature in a semiconductor device by blanket deposition of a first barrier layer over an anisotropically etched feature to prevent diffusion of metal into the substrate; filling the anisotropically etched feature with a metal to form a metal filled feature; planarizing the substrate surface to form an exposed surface of the metal filled feature; and depositing a second barrier layer to cover the exposed surface of the metal filled feature to form a capping layer. *See*, e.g., column 3, lines 37-53 of Tu. Thus, Tu does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch.

Further, Chang '240 is directed to a process for the in-situ nitridation and formation of metal salicides. Change '240 discloses accomplishing its objective to form metal salicides by utilizing a plasma generator. However, Chang '240 does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Ballanace discloses utilizing a "showerhead" for accomplishing a multi-zone gas flow control into a substrate in a process chamber. In accomplishing this objective, Ballance discloses a first gas distribution system which delivers a first gas to a first subset

of injection ports for injection into the chamber, and a second gas distribution system which delivers a second gas to a second subset of injection ports for injection into the chamber. However, Ballance does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Aronowitz discloses a process where a uniform amount of silicon oxide can be removed from a surface of an oxide previously formed over a semiconductor substrate by exposing the oxide to a nitrogen plasma in an etch chamber while applying an RF bias to the substrate support in the etch chamber. However, Aronowitz does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Moreover, Chang '964 discloses a method for determining a composition of an integrated circuit feature on a substrate, including collecting intensity data representative of spectral wavelengths of radiant energy generated by a plasma during plasma nitridation of the integrated circuit feature on the substrate, and analyzing the intensity data to determine a peak intensity at one of the wavelengths. However, Chang '964 does not remotely suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch. Thus, independent claims 1, 8 and 15 are patentably distinguishable over each primary reference Colombo, Alers, or Tu singly, or in any of their respective combinations with secondary references Chang '240, Ballance, Aronowitz, or Chang '964. Moreover, the fact that the Examiner has had to rely on a large number of references, i.e. seven (7) references, to argue for obviousness of the

independent claims itself indicates that the pending independent claims are not obvious in light of the cited art.

For the foregoing reasons, Appellants respectfully submit that the present invention, as defined by independent claims 1, 8, and 15 are patentably distinguishable over the cited references, either singly or in combination. Thus, claims 6 and 7 depending from independent claim 1, claim 14 depending from independent claim 8, and claims 16 and 19-20 depending from independent claim 15 are, *a fortiori*, also patentably distinguishable over the cited references for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejection of Claims 1, 6-8, 14-16, and 19-20 Under 35 USC §103(a) as Being Unpatentable Over Doyle in View of Alers, or Tu as Evidenced by Chang '240, or Ballance, or Aronowitz, or Chang '964.

Appellants respectfully submit that the present invention, as defined by independent claims 1, 8, and 15, is patentably distinguishable over the cited references, either singly or in combination.

Doyle discloses a method for increasing the dielectric constant of a gate dielectric by using a high dielectric constant material, such as a paraelectric material, instead of silicon dioxide. First, nitrogen is implanted into the silicon through a sacrificial oxide layer. After annealing the substrate and stripping the sacrificial oxide, a dielectric layer is formed from a material with a high dielectric constant, such as a paraelectric material.

Although the paraelectric material provides a source of oxygen for oxidation of silicon in subsequent high temperature process steps, Doyle claims that no oxidation takes place due to the presence of the nitrogen in the silicon. Therefore, there is no undesired decrease in the overall capacitance of the dielectric. When a gate electrode is formed on the dielectric layer, a nitrogen implant into the gate electrode can be used to prevent oxidation at the upper interface of the gate dielectric. *See*, e.g., column 2, line 48 through column 3, line 44 of Doyle. However, Doyle does not suggest that the processes of etching the gate stack and the nitridation of the etched gate stack are performed in a single plasma chamber. Moreover, as discussed above, use of a single plasma nitridation process chamber is not suggested by Alers or Tu, or their combination with Chang '240, Ballance, Aronowitz, or Chang '964. Thus, independent claims 1, 8 and 15 are patentably distinguishable over each primary reference Alers or Tu singly, or in any of their respective combinations with secondary references Chang '240, Ballance, Aronowitz, or Chang '964. Moreover, the fact that the Examiner has had to rely on a large number of references, i.e. six (6) references, to argue for obviousness of the independent claims itself indicates that the pending independent claims are not obvious in light of the cited art.

For the foregoing reasons, Appellants respectfully submit that the present invention, as defined by independent claims 1, 8, and 15 are patentably distinguishable over the cited references, either singly or in combination. Thus, claims 6 and 7 depending from independent claim 1, claim 14 depending from independent claim 8, and claims 16

and 19-20 depending from independent claim 15 are, *a fortiori*, also patentably distinguishable over the cited references for at least the reasons presented above and also for additional limitations contained in each dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention as defined by independent claims 1, 8, and 15 and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 6-8, 14-16, and 19-20 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 6-8, 14-16, and 19-20 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 4/25/06

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Date of Deposit: 4/25/06

Christina Carter
Name of Person Mailing Paper and/or Fee

Christina Carter 4/25/06
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 1: A method for forming a field-effect transistor on a substrate, said substrate including a high-k dielectric layer situated over said substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising steps of:

etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment;

performing a nitridation process on said gate stack, said nitridation process utilizing a nitrogen containing plasma to nitridate sidewalls of said gate stack, said nitridation process on said gate stack causing nitrogen to enter said high-k dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber, said plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack.

Claim 6: The method of claim 1 wherein said high-k dielectric segment is selected from the group consisting of hafnium oxide, hafnium silicate, zirconium oxide, zirconium silicate, and aluminum oxide.

Claim 7: The method of claim 1 wherein said gate electrode segment comprises polysilicon.

Claim 8: A method for forming a field-effect transistor on a substrate, said substrate including a high-k dielectric layer situated over said substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising a step of etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment, said method being characterized by:

selecting said high-k dielectric segment from the group consisting of hafnium oxide, hafnium silicate, zirconium oxide, zirconium silicate, and aluminum oxide;

performing a nitridation process on said gate stack;

said nitridation process utilizing a nitrogen containing plasma to nitridate sidewalls of said gate stack, said nitridation process on said gate stack causing nitrogen to enter said high-k dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber, said plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack.

Claim 14: The method of claim 8 wherein said gate electrode segment comprises polysilicon.

Claim 15: A method for forming a field-effect transistor on a substrate, said substrate including a high-k dielectric layer situated over said substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising steps of:

etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment, said gate stack comprising sidewalls;

utilizing a nitrogen plasma to nitridate said sidewalls of said gate stack;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber, said plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack;

forming source/drain regions adjacent to said gate stack;

fabricating spacers on said sidewalls of said gate stack;

performing a rapid thermal anneal on said gate stack.

Claim 16: The method of claim 15 wherein said step of utilizing said nitrogen plasma to nitridate said sidewalls of said gate stack causes nitrogen to enter said high-k

dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment.

Claim 19: The method of claim 15 wherein said high-k dielectric segment is selected from the group consisting of hafnium oxide, hafnium silicate, zirconium oxide, zirconium silicate, and aluminum oxide.

Claim 20: The method of claim 15 wherein said gate electrode segment comprises polysilicon.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Effective on 12/8/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

	Complete if Known
Application Number	10/705,347
Filing Date	11/08/2003
First Named Inventor	Labelle
Examiner Name	CHEN, Kin Chan
Art Unit	1765
Attorney Docket No.	0180151

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	$500.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: **50-0731** Deposit Account Name: **Farjami & Farjami LLP**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	0	x $50.00	= $ 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	0	x $200.00	= $ 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
$360.00	

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	0	/ 50 = 0 (round up to a whole number)	x $250.00 =	$ 0.00

4. OTHER FEE(S)

	Fees Paid($)
Non-English Specification, $130 fee (no small entity discount)	
Other: **Filing a brief in support of an appeal**	**$500.00**

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 38135	Telephone (949) 282-1000
Name (Print/Type)	Michael Farjami, Esq.		Date 4/25/06